Two New Modulation Strategies for Two-Stage Matrix Converter under Nonsinusoidal Input Voltages

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***Abstract*- For the two-stage matrix converter (TSMC) having no energy storage elements, the nonsinusoidal supply voltages will disturb the output voltage and result in low order harmonics. To compensate the output voltages, two new space vector modulation strategies are presented. One works with the rectifier stage, and the other with the inverter stage. The maximum transfer ratio under nonsinusoidal input is obtained by detecting the minimum amplitude of the nonsinusoidal input vector. Theoretical analysis and simulation results indicate that the output voltage is sinusoidal, and at the same time, the input current harmonics decrease.**

I. INTRODUCTION

The two-stage matrix converter (TSMC) is a direct frequency converter. Operating under the space vector PWM, it has the same input/output characters with the conventional matrix converter (CMC), such as a compact structure, sinusoidal input/output waveforms, adjustable input power factor, and variable magnitude variable frequency output voltage. Besides these, the TSMC has more advantages compared to the CMC in [1][2]. One of the most important is the zero-current commutation, with which the commutation of TSMC becomes easier and safer, and the losses of rectifier switches are reduced to a small amount.

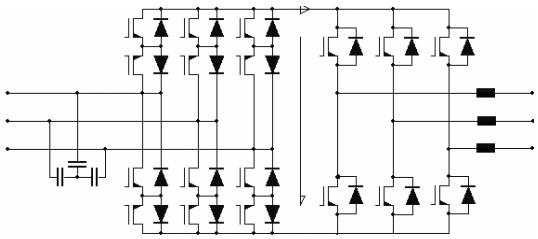

Fig.1. The TSMC topology

In the application of the TSMC, the input voltages usually contain harmonics. For the TSMC having no energy storage elements, the nonsinusoidal supply voltages will disturb the output voltage and result in low order harmonics. The same problem exists in the CMC. Because the modulation strategies of the CMC and TSMC are similar, the solutions of the CMC can be also useful or applied to the TSMC.

Some approaches to reduce the influence of nonsinusoidal supply voltages have been reported [3]-[9]. They are all feed-forward compensation, and [3]-[8] are for CMC, while [9] is for TSMC.

In [3]-[6], the input current disturbances under unbalanced supply voltages were analyzed. The optimized displacement angle of input current was dynamically modulated as a function of positive and negative sequence components of the input voltages. Balanced output voltages and optimized input current waveforms can be generated. In [7], the same method was used, but the key equations were not apparently similar to those in [3]. In fact, if the equations were rewritten in the same kind of parameters to represent the modulation strategy, the result would be the same. [3]-[7] deal with the problems caused by only negative sequence component, but the input harmonics, which exist in the actual supply voltages all the time, are not concerned.

In [8], nonsinusoidal input voltages were considered. And this time, the optimized displacement angle of input current was dynamically modulated as a function of fundamental positive sequence components of the input voltages. This approach led to the lowest value of the global input current distortion factor. However, the output voltages are not discussed.

In [9], a compensation method for the TSMC was presented. The sinusoidal output voltage was generated with nonsinusoidal input voltages. It was an approximate solution by omitting a part of the distortion in DC-link. But if the total harmonic distortion of the input voltages is large, the approximate solution would product harmonics in both output voltages and input currents.

In this paper, the switch function vectors of the TSMC are represented as the fundamental components and the harmonics. To obtain the sinusoidal output voltages, two new compensation strategies are introduced. Theoretical analysis illustrates that the qualities of the output voltages and input current produced by the two strategies are the same. The maximum transfer ratio under nonsinusoidal input is analyzed and obtained by detecting the minimum amplitude of the input voltage vector. Numerical simulation is presented to verify the theoretical analysis.

II. MODULATION

Assuming that the TSMC uses ideal switches, thus the input power flow equals to the output power flow at any instant, then

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$$P_i = P_o \tag{1}$$

Equation (1) can be further developed as

$$\vec{v}_i \bullet \vec{i}_i = \vec{v}_o \vec{i}_o \tag{2}$$

Suppose the load side is balanced, then the equation (2) demonstrates that under nonsinusoidal input voltages, in order to obtain harmonic-free output voltage/current, the input current must be nonsinusoidal, i.e. there're two goals for the feed-forward compensation: sinusoidal output voltages and sinusoidal input currents. Between them, the former is more important.

Any voltages can be represented as their fundamental positive sequence components and the harmonics. Hence using the Park Transformation, the vectors of nonsinusoidal input voltages can be represented as

$$\vec{v}_i = \vec{v}_p + \Delta\vec{v}_i \tag{3}$$

Where, $\vec{v}_i, \vec{v}_p, \Delta\vec{v}_i$ are the vectors of input voltages, input fundamental positive sequence component, and the harmonics respectively.

The vector of input fundamental positive sequence component can be represented as

$$\vec{v}_p = V_p e^{j(w_i t + \alpha)} \tag{4}$$

Where, V_p is the amplitude of input fundamental positive sequence voltages, w_i is the angular velocity, and α is the initial angle.

Similar to the equation (3), the vector of switch the function of rectifier stage can also be represented as its fundamental positive sequence components and the harmonics.

$$\vec{S}_{rec} = \vec{S}_{rp} + \Delta\vec{S}_{rec} \tag{5}$$

Where, $\vec{S}_{rec}, \vec{S}_{rp}, \Delta\vec{S}_{rec}$ are the vectors of the switch function of rectifier stage, its fundamental positive component, and the harmonics respectively.

As to the inverter stage, the similar definition is shown in (6).

$$\vec{S}_{inv} = \vec{S}_{ip} + \Delta\vec{S}_{inv} \tag{6}$$

Where, $\vec{S}_{inv}, \vec{S}_{ip}, \Delta\vec{S}_{inv}$ re the vectors of the switch function of inverter stage, its fundamental positive component, and the harmonics respectively.

The switch function vector of the fundamental positive component of rectifier/inverter stage can be expressed as

$$\vec{S}_{rp} = m_{rec} e^{j(w_i t + \alpha - \varphi_i)} \tag{7}$$

$$\vec{S}_{ip} = m_{inv} e^{j(w_o t + \varphi_o)} \tag{8}$$

Where, m_{rec} and m_{inv} are the modulation indices, and φ_i, φ_o are the displacement angles of the input current and output voltage respectively.

The DC-link voltage/current can be represented as

$$V_{DC} = \vec{S}_{rec} \cdot \vec{v}_i \tag{9}$$

$$I_{DC} = \vec{S}_{inv} \cdot \vec{i}_o \tag{10}$$

The output voltage/current can be represented as

$$\vec{v}_o = \vec{S}_{inv} \cdot V_{DC} \quad 11)$$

$$\vec{i}_i = \vec{S}_{rec} \cdot I_{DC} \tag{12}$$

It should be noted that four parameters in equation (5)~(8), which are m_{rec}, $\Delta\vec{S}_{rec}$, m_{inv} and $\Delta\vec{S}_{inv}$ can be controlled. So according to (5)~(12), there're two ways to obtain sinusoidal output voltages. The first way is to adjust m_{rec} and $\Delta\vec{S}_{rec}$ to obtain a constant DC-link voltage V_{DC}, and then the inverter stage can be modulated as the conventional DC/AC converters. The second way is, if V_{DC} is variable, to adjust m_{inv} and $\Delta\vec{S}_{inv}$.

A. Adjusting the Rectifier Stage

Combining (3), (4), (5), (7) and (9), the DC-link voltage can be represented as

$$\begin{aligned} V_{DC} &= m_{rec} V_p \cos(\varphi_i) \quad \vec{S}_{rec} \quad V_p e^{j(w_i t + \alpha)} \\ &+ m_{rec} \Delta\bullet\Delta^{j(w_i t + \alpha - \varphi_i)} \quad \vec{v}_i \quad \vec{S}_{rec} \quad v_i \end{aligned} \tag{13}$$

For the existence of different order harmonics, the last three terms in (13) are variable. Suppose the constant value of m_{rec}, the only constant is the first term. Hence the demanded DC-link voltage can be represented as

$$V_d = m_{rec} V_p \cos(\varphi_i) \tag{14}$$

Combining (9) and (14), the switch function vector of the rectifier stage is shown in (15).

$$\vec{S}_{rec} = \frac{m_{rec} V_p \cos(\varphi_i)}{|\vec{v}_i|} \angle v_i \tag{15}$$

Where, $0 < m_{rec} \le 1$. V_p, φ_i, $|\vec{v}_i|$ and $\angle\vec{v}_i$ can be obtained from the detection of three phase input voltages. So, $\vec{S}_{rec}$ can be fully decided.

With the constant DC-link voltage, the switch function vector of the inverter stage can be simplified as

$$\vec{S}_{inv} = \vec{S}_{ip} \quad m_{inv} e^{j(w_o t + \varphi_o)} \tag{16}$$

Where, $0 < m_{inv} \le 1$, and m_{inv} should be preseted.

Hence combining (12), (14) and (16), the output voltage vector can be represented as

$$\vec{v}_o = m_{inv} m_{rec} V_p \cos(\varphi_i) e^{j(w_o t + \varphi_o)} \tag{17}$$

The result illustrates that the corresponding output voltage is sinusoidal and contains no any harmonics.

Assuming the load is balanced, the output current vector can be represented as

$$\vec{i}_o = I_o e^{j(w_o t + \beta)} \tag{18}$$

Combining (10) (16)and (18), the DC-link current can be represented as

$$I_{DC} = m_{inv} I_o \cos(\varphi_o - \beta) \tag{19}$$

It can be seen that the DC-link current is a constant.

Substituting (15) and (19) into (12), the input current is obtained in (20).

$$\vec{i}_i = m_{rec} m_{inv} V_p I_o \cos(\varphi\beta\varphi \quad)\cos(\quad_i) \frac{\angle\vec{v}_i}{|\vec{v}_i|} \tag{20}$$

The displacement angle of input current can be calculated in (21).

$$\overrightarrow{v_i} \bullet \overrightarrow{i_i} = \cdot p \ \cos(\varphi_i) \tag{21}$$

Where, $p = m_{rec} m_{inv} V_p I_o \cos(\varphi\beta \quad)$. So, the displacement angle of input current is φ_i.

The strategy in [9] is similar with the strategy A, but it's an approximate solution by neglecting the high order parts in (13). When the total harmonic distortion of the input voltages is large, the high order parts couldn't be ignored.

B. Adjusting the Inverter Stage

If the DC-link voltage is variable, the equation (13) can be simplified as

$$V_{DC} = V_d + \Delta V_d \quad m_{rec} V_p \cos(\varphi_i) \quad V_d \tag{22}$$

Substituting (6) and (22) into (11) leads to

$$\begin{aligned} \overrightarrow{v_o} &= m_{inv} V_d e^{j(w_o t + \varphi_o)} \quad S_{inv} \quad V_d \\ &+ m_{inv} \Delta V_d e^{j(w_o t + \varphi_o)} \quad V_d \quad \overrightarrow{S_{inv}} \quad V_d \end{aligned} \tag{23}$$

Considering that the last three terms in (23) are harmonics, and assuming the constant value of m_{inv}, the demanded output voltage vector can be represented as

$$\overrightarrow{v_o} = m_{inv} V_d e^{j(w_o t + \varphi_o)} \tag{24}$$

Combining (11) and (24), the switch function vector of the inverter stage is shown in (25).

$$\overrightarrow{S_{inv}} = \cdot \overrightarrow{S_{ip}} \ \frac{V_d}{V_{DC}} \tag{25}$$

Where, $\overrightarrow{S_{ip}} = m_{inv} e^{j(w_o t + \varphi_o)}$; $V_{DC} = \overrightarrow{S_{rec}} \bullet \overrightarrow{v_i}$. Hence (25) can be changed as

$$\overrightarrow{S_{inv}} = \cdot m_{inv} e^{j(w_o t + \varphi_o)} \ \frac{m_{rec} V_p \cos(\varphi_i)}{\overrightarrow{S_{rec}} \bullet \overrightarrow{v_i}} \tag{26}$$

With the detection of three phase input voltages, $\overrightarrow{S_{inv}}$ can be fully decided.

Assuming the load is balanced, the output current representation in (18) can be used. Substituting (10), (18) and (26) into (12), the input current can be represented as

$$\vec{i}_i = m_{rec} m_{inv} V_p I_o \cos(\varphi\beta\varphi \quad) \cos(\ _i) \ \frac{\angle \overrightarrow{v_i}}{\left|\overrightarrow{v_i}\right|} \tag{27}$$

Comparing (17) with (24), (21) with (27), it can be easily seen that the output voltages and input currents are the same. Meanwhile, the strategies described in *A* and *B* have the same input/output characteristics. The key difference between the two strategies is that the switch function derived in (26) is more complex than those in (15) and (16). It should be noted that the following discussion will be based on the former strategy because it is easier to do in the application.

C. Maximum Transfer Ratio

Unlike the unbalance systems, the maximum transfer ratio can't be calculated easily. Prediction can be done by detecting and calculating the maximum of input voltages vectors.

Equation (15) can be developed as the amplitude equation:

$$\left|\overrightarrow{S_{rec}}\right| = \frac{m_{rec} V_p \cos(\varphi_i)}{\left|\overrightarrow{v_i}\right|} \tag{28}$$

To get the maximum transfer ratio, i.e. the maximum $\left|\overrightarrow{S_{rec}}\right|$, two constraint conditions can be set as m_{rec} =1 and $\cos(\varphi_i)$ =1.

It can be obtained that $V_p \Big/ \left|\overrightarrow{v_i}\right| \le 1$, for $\left|\overrightarrow{S_{rec}}\right| \le 1$. The trajectory of $\overrightarrow{v_i}$ is shown in Fig.2.

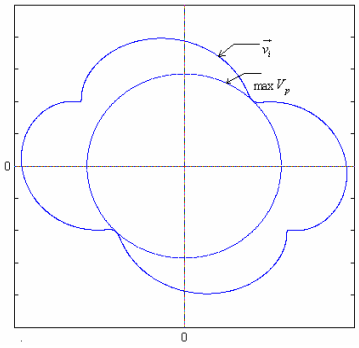

Fig.2 Trajectory of $\overrightarrow{v_i}$

Because $\left|\overrightarrow{v_i}\right|$ is a variable for the nonsinusoidal voltages, V_p couldn't be the maximum amplitude of the fundamental positive sequence component. Otherwise the condition $V_p \Big/ \left|\overrightarrow{v_i}\right| \le 1$ can't be satisfied. Its range is shown as

$$V_p \le \min \left|\overrightarrow{v_i}\right| \tag{29}$$

The maximum transfer ratio can be obtained while (30) is satisfied.

$$V_p = \min \left|\overrightarrow{v_i}\right| \tag{30}$$

III. SIMULATION

To illustrate the modulation strategies presented in the previous section, the simulation has been carried out under nonsinusoidal supply voltages. The parameter is defined as

Input frequency: 50 Hz;
Output frequency: 80Hz;
Input voltage (phase-to-ground):
Fundamental positive sequence: $220\sqrt{2}\angle 0^\circ$ V,
Fundamental negative sequence: $30.8\sqrt{2}\angle 35^\circ$ V,
5th order positive sequence harmonic: $33\sqrt{2}\angle -25^\circ$ V.

Fig.3 shows that without compensation the output voltage and input current are nonsinusoidal. Their FFT analyses (see Fig.4) illustrate that there're a great lot of low order harmonics. The THD (total harmonic distortion) is very high.

Using either the modulation strategy A or B, the results are presented in Fig.5. During the first 0.02 second, i.e. one input voltage period, 3-phase instantaneous input voltages are detected. Then the minimum amplitude of the input voltage vector and the phase of the fundamental positive sequence components can be calculated.

The corresponding minimum amplitude of the input voltage vector is 285.59V, and if the input voltage contains only fundamental positive sequence component ($220\sqrt{2}\angle 0^{\circ}$ V), that amplitude should be 381.05V. Hence, the transfer ratio is decreased for the nonsinusoidal input voltages.

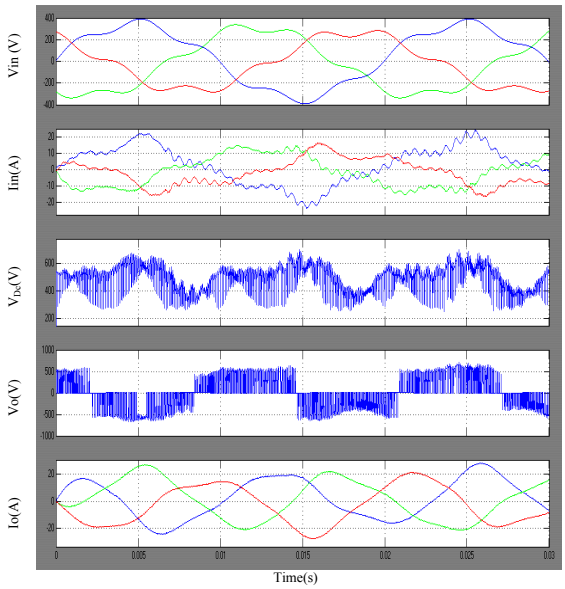

Fig.3 Simulation results of TSMC without compensation

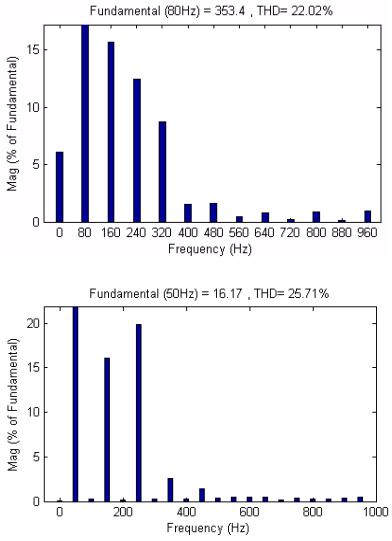

Fig.4 FFT analyses for output voltage and input current without compensation

The output voltage and the input current in Fig.5 are sinusoidal. Their FFT analyses (see Fig.6) illustrate that both the THD and the low order harmonics of the output voltage are decreased largely. The low order harmonics of the input current remain very high, and according to the analyses about power balance in (1) and (2), it's reasonable. It can be seen that the THD of the input current is decreased.

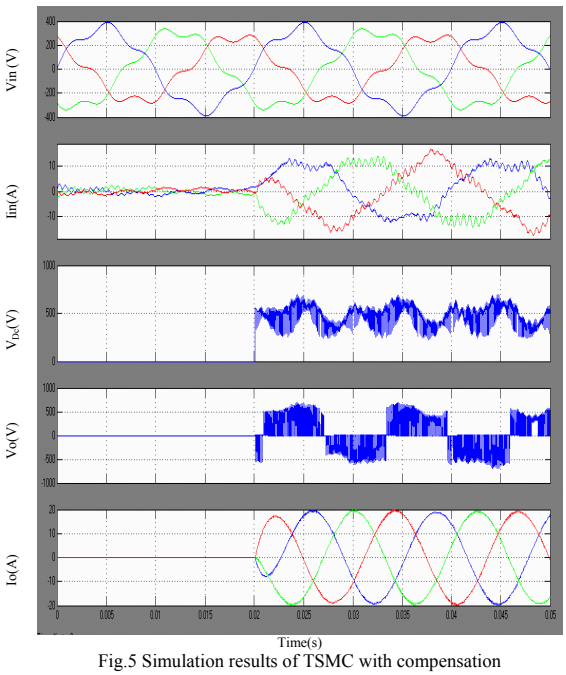

Fig.5 Simulation results of TSMC with compensation

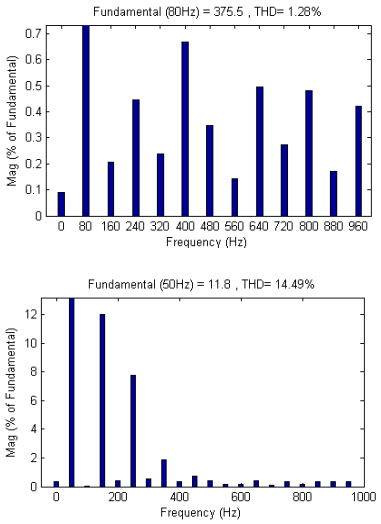

Fig.6 FFT analyses for output voltage and input current with compensation

IV. CONCLUSIONS

The first goal of this paper is to obtain sinusoidal output voltage for the TSMC operating under nonsinusoidal input.

The switch function vectors of the TSMC are represented as the fundamental components and the harmonics. With this representation, two modulation strategies can be obtained easily. Their input/output analyses illustrate that the characteristics of the two strategies are the same.

For the existence of the harmonics of the nonsinusoidal input voltage, only partial vector of the input voltage can be used to synthesize the output vector. The maximum transfer ratio under nonsinusoidal input is analyzed and obtained by detecting the minimum amplitude of the input voltage vector.

The simulation results of the TSMC operation under nonsinusoidal input voltages have illustrated that the output voltage was sinusoidal, and at the same time, the quality of the input current was improved.

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